Claims

What is claimed is:

1. A processing system comprising:

first processing circuitry for performing a first function;

first memory circuitry, coupled to the first processing circuitry, for storing received packets, at least a portion of the packets stored by the first memory circuitry being usable by the first processing circuitry in accordance with the first function;

at least second processing circuitry for performing a second function; and

at least second memory circuitry, coupled to the second processing circuitry, for storing at least a portion of the same packets stored in the first memory circuitry, at least a portion of the packets stored in the second memory circuitry being usable by the second processing circuitry in accordance with the second function.

2. The system of claim 1 wherein the first processing circuitry, the first memory circuitry, the second processing circuitry and the second memory circuitry are implemented on the same integrated circuit.

3. The system of claim 1 wherein the first processing circuitry and the first memory circuitry are implemented on a first integrated circuit, and the second processing circuitry and the second memory circuitry are implemented on a second integrated circuit.

4. The system of claim 1 wherein the first function and the second function are performed in accordance with the same integrated circuit.

5. The system of claim 1 wherein the first function and the second function are performed in accordance with different integrated circuits.

6. The system of claim 1 wherein the first processing circuitry and the first memory circuitry comprise a network processor.

7. The system of claim 6 wherein the first function comprises a packet classifying operation.

8. The system of claim 1 wherein the second processing circuitry and the second memory circuitry comprise a traffic manager.

9. The system of claim 8 wherein the second function comprises a packet scheduling operation.

10. The system of claim 1 further comprising:

first reassembly circuitry, coupled to the first memory circuitry, for reassembling subsets of received packets prior to storing the packets in the first memory circuitry; and

at least second reassembly circuitry, coupled to the second memory circuitry, for reassembling at least a portion of the same subsets of packets reassembled by the first reassembly circuitry, prior to storing the packets in the second memory circuitry.

11. The system of claim 10 further comprising parsing circuitry, coupled to the first reassembly circuitry and the second reassembly circuitry, for parsing information from the received packets for use by the first reassembly circuitry and the second reassembly circuitry in respectively reassembling the packets.

12. The system of claim 10 wherein the packet subsets are cells.

13. The system of claim 1 wherein the first processing circuitry and the second processing circuitry operate in a packet switching device.

14. The system of claim 13 wherein the first processing circuitry and the second processing circuitry operate between a packet network interface and a switch fabric of the packet switching device.

15. A method for use in a processing system wherein the processing system is responsive to packets, the method comprising the steps of:

reassembling subsets of received packets into reassembled packets in a first reassembler; and

storing the reassembled packets in a first memory, at least a portion of the reassembled packets stored by the first memory being usable by a first processor in accordance with a first function;

wherein at least a portion of the subsets of received packets reassembled by the first reassembler may be reassembled in at least a second reassembler for storage in at least a second memory usable by at least a second processor in accordance with a second function.

16. The method of claim 15 wherein the first reassembler, the first processor, the first memory, the second reassembler, the second processor and the second memory are implemented on the same integrated circuit.

17. The method of claim 15 wherein the first reassembler, the first processor and the first memory are implemented on a first integrated circuit, and the second reassembler, the second processor and the second memory are implemented on a second integrated circuit.

18. Apparatus for use in a processing system wherein the processing system is responsive to packets, the apparatus comprising:

a first memory; and

a first processor operative to: (i) reassemble subsets of received packets into reassembled packets; and (ii) cause the storage of the reassembled packets in the first memory, at

least a portion of the reassembled packets stored by the first memory being usable in accordance with a first function;

wherein at least a portion of the subsets of received packets reassembled by the first reassembler may be reassembled by at least a second processor for storage in at least a second memory usable in accordance with a second function.

19. The apparatus of claim 18 wherein the first processor and the first memory, the second processor and the second memory are implemented on the same integrated circuit.

20. The apparatus of claim 18 wherein the first processor and the first memory are implemented on a first integrated circuit, and the second processor and the second memory are implemented on a second integrated circuit.